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06EC45

Fourth Semester B.E. Degree Examination, June/July 2013

Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the behavioral, structural and dataflow description types in HDL programming with examples. **(12 Marks)**

b. Explain the following data types:
i) Physical, std_logic in VHDL ii) Nets, registers in verilog **(08 Marks)**

2 a. Write HDL code for 2 × 1 multiplexer with active low enable. Show its simulation waveform. **(08 Marks)**

b. Write HDL code for 2 × 2 unsigned combinational array multiplier. Show its gate level diagram and simulation waveform. **(12 Marks)**

3 a. Write VHDL code for 3 bit binary counter with active high synchronous clear in behavioral description show excitation table and simulation waveform. **(10 Marks)**

b. Write VHDL and verilog code for calculating the factorial using behavioral description with while – loop. **(10 Marks)**

4 a. Explain binding between:
i) Entity and architecture
ii) Entity and component in VHDL. **(08 Marks)**

b. Write VHDL code of a 2 × 4 decoder with tri-state output in structural description. Show logic diagram and simulation waveform. **(12 Marks)**

PART – B

5 a. What are procedures in VHDL? Explain the need for procedures. **(05 Marks)**

b. Write VHDL code for a full adder using procedure and task. **(10 Marks)**

c. Write VHDL code to find the greater of two signed numbers using function. **(05 Marks)**

6 a. Explain how to attach package to the VHDL module. Give an example. **(08 Marks)**

b. Why mixed type description is needed? Explain. **(04 Marks)**

c. Write HDL description code of 16 × 8 SRAM. **(08 Marks)**

7 a. Explain how to invoke a VHDL entity from a verilog module. Give an example. **(10 Marks)**

b. Write HDL code for a Master Slave D flip-flop in mixed language description. Show simulation waveform. **(10 Marks)**

8 a. Write flow chart of synthesis steps and explain. **(10 Marks)**

b. Write HDL code for signal assignment statement y = 2 * x + 3. Show the synthesized logic symbol and gate level diagram. **(10 Marks)**

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